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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,886	08/26/2003	Monte Manning	MI22-2374	4873

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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER

NADAV, ORI

ART UNIT PAPER NUMBER

2811

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/648,886	Applicant(s) MANNING, MONTE	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 40-58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 40-58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/29/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 40-58 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification recites first and second conductive lines being electrically isolated from one another laterally by intervening insulating spacers. There is no support for the claimed limitations of first conductive lines being electrically isolated from the second conductive lines, as recited in claims 40, 48 and 56.

The specification and figure 10 describe an electrically insulative oxide material 60 on and in contact with respective first series conductive line 36. There is no support for the claimed limitations of electrically insulative oxide material on and in contact with respective first series conductive lines, as recited in claim 56.

There is no support for the claimed limitations of individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with the electrically insulating oxide material over the respective individual first series conductive lines, as recited in claim 56.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains: Patentability shall not be negated by the manner in which the invention was made.

Claims 40-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (5,413,962) in view of Choe (5,583,357).

Lur et al. teach in figure 11 and related text an Integrated circuitry comprising:

- a semiconductive substrate 20;
- an electrically insulating layer 30 over the semiconductive substrate;
- a series of alternating first and second conductive lines 40 spaced and positioned laterally adjacent one another directly over the insulating layer 30, the first lines and the second lines having respective line tops, and
- intervening insulating spacers laterally between the first and second conductive lines, the spacers having respective spacer tops that are substantially coplanar with at least some of the first and second line tops, the first conductive lines being electrically laterally isolated from the second conductive lines, and the series of first or second conductive lines can provide cross talk shielding for the other series.

Lur et al. do not explicitly state that the spacers are insulating spacers, and that the first conductive lines are electrically isolated from the second conductive lines such that the series of first or second conductive lines provide cross talk shielding for the other series.

Choe teaches in figure 11A and related text insulating spacers 5. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use insulating spacers and to electrically isolate the first conductive lines from the second conductive lines such that the series of first or second conductive lines provide cross talk shielding for the other series in Lur et al.'s device in order to provide protection for the device, and in order to use the device in an application which requires cross talk shielding.

Regarding claims 41 and 49, Lur et al. teach in figure 11 and related text at least some of the individual laterally adjacent first and second series lines are disposed directly on the electrically insulating layer.

Regarding claims 42 and 50, Lur et al. teach in figure 11 and related text the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, wherein Choe teaches in figure 11A and related text first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape in Lur et al.'s device in order to simplify the processing steps of making the device by forming the lines at constant intervals.

Art Unit: 2811

Regarding claims 43 and 51, Lur et al. teach in figure 11 and related text the first and second conductive lines constitute the same materials.

Regarding claims 44, 46, 52 and 54, Lur et al. teach in figure 11 and related text the first 24 and second 40 conductive lines constitute different materials, wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal. Note that the broad recitation of the claim does not require that all the series of alternating first and second conductive lines being located directly over the insulating layer.

Regarding claims 45 and 53, Lur et al. do teach in figure 11 first conductive lines predominately comprise undoped polysilicon. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first conductive lines predominately comprise undoped polysilicon in Lur et al.'s device in order to adjust the conductivity of the lines according to the application at hand.

Regarding claims 47 and 55, Lur et al. teach in figure 11 and related text a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

Regarding claim 48, Lur et al. teach in figure 11 and related text first and second lines having respective lateral widths and being spaced and positioned laterally adjacent one

Art Unit: 2811

another, the first lines and the second lines being electrically isolated and separated from one another laterally by intervening strips of spacer material only having respective individual material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines, and none of the first and second lines overlapping any immediately laterally adjacent first or second lines.

Claims 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu (5,519,239) in view of Miyanaga et al. (5,418,187) and Okummura et al. (4,984,055).

Regarding claim 56, Chu teaches in figure 3O and related text an Integrated circuitry comprising:

- a semiconductive substrate 300;

- a series of first conductive lines 302, 303 (see figure 3H) over the substrate, the first series conductive lines having individual pairs of respective sidewalls;

- electrically insulative oxide material 312 over respective first series conductive lines, a top of the oxide material over at least some of the lines defining a first plane;

- a plurality of insulative oxide sidewall spacer pairs 311, individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with the electrically insulating oxide material over the respective individual first series conductive lines; individual first series conductive lines being effectively insulated by the gate oxide layer 301, the respective sidewall spacer pairs 311, and the respective insulating oxide material; and

a series of second conductive metal-containing lines 313 having respective line tops at least some of which define a second plane that is coplanar with said first plane, the series of second conductive lines being over the substrate.

Chu does not teach an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate, metal conductor comprising aluminum, and a gate not including a dedicated dielectric layer thereon such that the electrically insulative oxide material is on and in contact with respective first series conductive lines and the first conductive lines are electrically isolated from the second conductive lines.

Miyanaga et al. teach in figure 1E and related text an electrically insulative borophosphosilicate glass (BPSG) layer 11 over the semiconductive substrate 100 and metal conductor comprising aluminum.

Okumura et al. teach in figure 12 and related text a gate 9 not including a dedicated dielectric layer thereon such that the electrically insulative oxide material 12 is on and in contact with respective first series conductive lines.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a metal conductor comprising aluminum and an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate of Chu's device in order to reduce the contact resistance of the device, to promote surface tension, to obtain higher yield and reliability, to simplify the processing steps of making the device and in order to use the device in an application which requires electrically isolate conductive lines, respectively. The combination is motivated by the teachings of Miyanaga et al. who point out the advantages of using an electrically insulative

Art Unit: 2811

borophosphosilicate glass (BPSG) layer over the semiconductive substrate (column 2, lines 13-68, and column 9, lines 5-12).

Regarding claim 57, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first series conductive lines having elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms in Chu's device, since it is within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 58, Chu teaches in figure 30 and related text individual second series lines have substantially a common lateral cross sectional shape.

Response to Arguments

Applicant argues that the polysilicon conductors 24 of Lur et al. are not provided sufficiently laterally adjacent to provide cross-talk shielding.

Lur et al. teach conductors 24 being laterally next to (adjacent) to each other. The disclosure does not teach that at certain distance from each other the conductors can not provide cross-talk shielding. Therefore, the conductors of Lur et al. provide cross-talk shielding, as claimed.

The rest of applicant's arguments with respect to claims 40-58 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2811

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is (571) 272-1660. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is 308-0956

A handwritten signature in black ink, appearing to read 'Ori Nadav', is positioned above the printed name and title.

O.N.
6/3/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800